WHAT IS CLAIMED IS:

1. A method for precluding stress-induced void formation in a semiconductor component, comprising:

providing a semiconductor substrate; and

forming a first portion of a metallization system above the semiconductor substrate, the first portion having a void preclusion feature.

2. The method of claim 1, wherein forming a first portion of the metallization system comprises:

disposing a layer of dielectric material over the semiconductor substrate;

forming at least one opening in the layer of dielectric material, wherein a portion of the layer of dielectric material remains adjacent the at least one opening and wherein the portion of the dielectric material that remains adjacent the at least one opening serves as the void preclusion feature; and

filling the at least one opening with an electrically conductive material.

3. The method of claim 2, wherein forming the at least one opening includes using an anisotropic reactive ion etch to form the at least one opening.

4. The method of claim 2, wherein the portion of the dielectric material that remains adjacent the at least one opening has a polygonal shape.

5. The method of claim 4, wherein the polygonal shape is selected from the group of polygonal shapes consisting of a square, a rectangle, a pentagon, a triangle, a hexagon, a heptagon, and an octagon.

6. The method of claim 2, wherein the portion of the dielectric material that remains adjacent the at least one opening has a circular shape.

7. The method of claim 1, further including forming a second portion of the metallization system, the second portion laterally spaced apart from the first portion.

8. The method of claim 7, further including coupling the first portion of the metallization system to the second portion of the metallization system with a third portion of the metallization system, wherein a width of the third portion of the metallization system is less than a width of the first and second portions of the metallization system.

9. The method of claim 7, further including coupling the first portion of the metallization system to the second portion of the metallization system with a third portion of the metallization system, wherein the first and second portions are separated from the semiconductor substrate by a first distance and the third portion is separated from the semiconductor substrate by a second distance.

10. The method of claim 9, wherein the second distance is less than the first distance.

11. A method for manufacturing a metallization system capable of precluding stress-induced void formation in a portion thereof, the method comprising:

providing a semiconductor substrate;

disposing a first portion of a conductive interconnect over the semiconductor substrate, the first portion having a width; and

forming a plurality of apertures in the first portion of the conductive interconnect.

12. The method of claim 11, further including disposing second and third portions of the conductive interconnect over the semiconductor substrate, the first and second portions spaced apart from the semiconductor substrate by a first distance and the third portion spaced apart from the semiconductor substrate by a second distance, the second distance different from the first distance.

13. The method of claim 11, wherein disposing the first, second, and third portions of the conductive interconnect comprises:

disposing a first layer of dielectric material over the semiconductor substrate;

forming a trench in the first layer of dielectric material;

filling the trench with electrically conductive material to form a filled trench that serves as the third portion of the conductive interconnect;

disposing a second layer of dielectric material over the filled trench;

forming a plurality of openings in the second layer of dielectric material, a first opening exposing a first portion of the filled trench and a second opening exposing a second portion of the filled trench; and

filling the plurality of openings with additional electrically conductive material, wherein electrically conductive material filling a first opening of the plurality of openings serves as the first portion of the conductive interconnect and the electrically conductive material filling a second opening of the plurality of openings serves as the second portion of the conductive interconnect.

14. The method of claim 11, wherein disposing the first, second, and third portions of the conductive interconnect comprises:

disposing a first layer of dielectric material over the semiconductor substrate;

forming first and second trenches in the first layer of dielectric material, the first and second trenches having dielectric pillars formed therein;

filling the first and second trenches with electrically conductive material to form the first and second portions of the conductive interconnect;

disposing a second layer of dielectric material over the first and second portions of the conductive interconnect;

forming a third trench, the third trench in the second layer of dielectric material;

forming first and second vias in the second layer of dielectric material, the first via exposing the first portion of the conductive interconnect and the second via exposing the second portion of the conductive interconnect; and

filling the third trench and the first and second vias with an electrically conductive material, wherein the electrically conductive material filling the first via electrically couples the first portion of the conductive interconnect to the third portion of the conductive interconnect and the electrically conductive material filling the second via couples the second portion of the conductive interconnect to the third portion of the conductive interconnect.

15. The method of claim 14, wherein forming the dielectric pillars includes forming square shaped dielectric pillars.

16. The method of claim 11, wherein forming the first, second, and third portions includes:

forming a first layer of dielectric material over the semiconductor substrate;

disposing an electrically conductive material over the layer of dielectric material;

forming the first and second portions of the conductive interconnect from the electrically conductive material;

forming at least one opening in each of the first and second portions of the conductive interconnect;

forming a second layer of dielectric material over the first and second portions of the conductive interconnect;

forming first and second openings in the second layer of dielectric material, the first opening exposing the first portion of the conductive interconnect and the second opening exposing the second portion of the conductive interconnect; and

disposing additional electrically conductive material over the second layer of dielectric material, the second layer of electrically conductive material filling the first and second openings in the second layer of dielectric material.

17. A semiconductor component, comprising:

a semiconductor substrate;

a layer of dielectric material disposed over the semiconductor substrate; and

a first portion of a metallization system over the layer of dielectric material, the first portion spaced apart from the semiconductor substrate by a first distance and having at least one aperture.

18. The semiconductor component of claim 17, further including a second portion of a metallization system coupled to the first portion of the metallization system, the second portion spaced apart from the semiconductor substrate by a second distance.

19. The semiconductor component of claim 18, wherein the second distance is less than the first distance.

20. The semiconductor component of claim 19, further including a third portion of the metallization system coupled to the second portion of the metallization system.

21. The semiconductor component of claim 20, wherein the third portion is spaced apart from the semiconductor substrate by a third distance.

22. The semiconductor component of claim 21, wherein the first distance is substantially equal to the third distance.